



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,332	11/08/2001	Hiroyuki Kiyoku	Q66212	5542

7590 07/05/2005

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, NW
Washington, DC 20037-3213

EXAMINER

ANDERSON, MATTHEW A

ART UNIT	PAPER NUMBER
----------	--------------

1722

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/986,332

Applicant(s)

KIYOKU ET AL.

Examiner

Matthew A. Anderson

Art Unit

1722

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 208-220, 235, 238 and 240-247 is/are pending in the application.
- 4a) Of the above claim(s) 221-233 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 208-220, 235, 238 and 240-247 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/202,141.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on 5/09/2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 208-213, 215, 217-220, 235, 238, 240-247, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (WO 97/11518) in view of in view of Takeuchi et al. (US 5,239,188) and Ohba et al. (US 5,656,832), and further in view of Harunori et al.(JP-07-201745).

4. The examiner has used the disclosure of US 6,377,596 B1 as a translation of the PCT publication of Tanaka et al.

Art Unit: 1722

Tanaka et al. discloses a method for growing a low defect monocrystalline defect monocrystalline layer over a mask. The method is described as forming light emitting diodes in col. 1 lines 15-25. In Fig. 16 and in col. 28 lines 34+ the method is described. Striped openings in a insulator mask are formed on the (0001) plane of a sapphire substrate. (in col. 19 lines 65 is suggested that such stripes be formed in the direction parallel to the (11-20) A plane of a sapphire substrate. Perpendicular stripes to the (11-20) plane are also disclose in col. 11 line 55.) A GaN buffer layer is formed in the spaces between the stripes. N-type GaN is grown from the spaces laterally until it covers the mask between them (i.e. coalesces). The growth is described as by MOVPE. The defect density obtained is disclosed in col. 32 as 10^4 to 10^5 defects per cm^2 . MOVPE is described in col. 17 and 18 in which a tri-methyl gallium is reacted with ammonia to form the GaN. The substrate is disclosed as sapphire (Al_2O_3) or SiC. The insulator making up the mask was disclosed in col. 5 lines 65+ and col. 6 lines 1-5 as amorphous material such as SiO_2 , Si_3N_4 , PSG, SION, or Ta_2O_3 . The relative size of the spaces is seen in Fig. 16 B to less than that of the mask layers. Multiple iterations of growth and mask layer formation are suggested in Figs. 16a-16c and 18a-18c. Further, and active layer (6) is grown on the second nitride semiconductor (5) as seen in Fig. 18C.

Tanaka et al, does not explicitly suggest a buffer layer or an off angled substrate as ways of reducing the defect density of the GaN epitaxial layer obtained.

Art Unit: 1722

Takeuchi et al. discloses a gallium nitride base semiconductor device. In Fig. 4A, 4B, 4C, and 4D is shown an epitaxial overgrowth of GaN on a Si substrate using an AlN mask layer. In Col. 3 lines 35-50, it is disclosed that the nitride semiconductor will also deposit on a thin AlN buffer layer on a sapphire substrate. In Fig. 3 is shown an n-GaN single crystal. In Fig. 4C is seen the growth of GaN from the sides of the recesses in the overlying AlN layer.

Ohba et al. discloses methods of growing nitride epitaxial layers with the use of buffer layers. Ohba et al. discloses (col. 6 lines 11-23) that growing a nitride layer on a buffer layer with the use of an inclined substrate with an angle of inclination of from 0.5 degrees to 10 degrees promotes higher quality growth and the ability to facilitate lateral crystal growth.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine the disclosures of the references cited to yield an improved method of forming a gallium nitride semiconductor because the use of nitride buffer layers (i.e. a nitride underlayer) on a sapphire substrate and inclined or off-angled substrates to reduce defects and promote lateral growth as well as use of mask layers for epitaxial overgrowth and recombination were known in the art. Motivation is the reduced defects and promotion of lateral growth and thus the expectation of a better product.

Tanaka combined as above does not explicitly suggest that the off-angled substrate be formed stepwise.

Harunori et al. discloses (see abstract) using a stepwise formation of a (0001) (a.k.a. the C plane) as a growth surface for GaN epitaxy.

Art Unit: 1722

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine and use Harunori's step wise off-angled substrate because such were known in the art to improve purity and crystallinity in epitaxy methods. Motivation is improved crystal.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the present invention to form a nitride semiconductor as disclosed in Claims 208, 211, 240, 243, because the use of nitride buffer layers (i.e. a nitride underlayer) on a sapphire (for example) substrate, the use of step-wise off-angled (explicitly 0.5 degrees which is less than 1 degree) substrates to reduce defects and the use of mask layers for epitaxial overgrowth and recombination, where known in the art to produce nitride semiconductors with reduced defect densities (i.e. high crystallinity) with high purity.

In respect to claims 208, 209, 210, 217-220, it would have been obvious to one of ordinary skill in the art at the time of the present invention to use multiple iterations of mask layers, position the second mask over the windows in the first mask, and to grow the first and second nitride semiconductors laterally on the growth masks to eventually recombine because Tanaka et al. suggests this in Figs . 16 and 18.

In respect to claim 212, it would have been obvious to one of ordinary skill in the art at the time of the present invention to grow light emitting diodes by this method because Tanaka et al. suggests this very use in col. 1 lines 15-25.

In respect to claim 213, it would have been obvious to one of ordinary skill in the art at the time of the present invention to include indium in the nitride

Art Unit: 1722

semiconductor being grown because Tanaka et al. suggests this in col. 23 lines 35-50.

In respect to claim 215, it would have been obvious to one of ordinary skill in the art to dope the first nitride semiconductor with an n-type impurity because such a doping was known in the art (Takeuchi et al.).

In respect to claim 235, 238, 241, 244 it would have been obvious to one of ordinary skill in the art at the time of the present invention to use a C-plane (i.e. that plane perpendicular to the (0001) direction) of a sapphire substrate because Ohba et al. discloses the C-plane of an off-angled sapphire substrate as useful for improving GaN epitaxial quality. (col. 6 lines 11-23)

In respect to claims 242, 245, 246-247, it would have been obvious to optimize the proportions of the step to achieve optimized results. Moreover, this mere adjustment of features to achieve optimum results is not patentable, nor will changes in form, proportions, or degree support patentability. (L.D. Scheiber Cheese Co. v. Clearfield Cheese Co., 214 USPQ 285).

5. Claims 214, 216 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of in view of Takeuchi et al. and Ohba et al., and further in view of Tischler et al.(US 5,679,152).

Tanaka combined is disclosed above.

Tanaka combined does not explicitly suggest using a superlattice buffer layer on the nitride substrate formed or Si doping to form n-type nitrides.

Art Unit: 1722

Tischler et al. discloses in column 4 lines 35-50 an alternately layered nitride superlattice to reduce the dislocation defects in a GaN crystals and alloys thereof. N-type GaN is disclosed as formed from Si additions in col. 8 lines 60+.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine the superlattice of Tischler et al. with Tanaka combined because then one of ordinary skill would have expected the product crystal to have fewer defects.

In respect to claim 214, it would have been obvious to one of ordinary skill in the art at the time of the present invention to form a buffer layer as claimed because such would have been expected to improve the nitride semiconductor grown thereon.

In respect to claim 216, it would have been obvious to one of ordinary skill in the art at the time of the present invention to form n-type nitrides with Si doping because such was known in the art (i.e. by Tischler et al.).

Response to Arguments

6. Applicant's arguments filed 6/09/2005 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Claims 208 and 217 are at least suggested by the

Art Unit: 1722

0.5' to 10' off-angle taught by Ohba et al. in col. 6 lines 10-25. (0.5 is less than 1.)

The argument that the drawing of Harunori's terraced substrate is quite different is not convincing. In view of the combination used above, the step-wise substrate is obvious and would have been expected to contribute to the quality of the crystal grown.

The argument that crystal defects are microscopic problems and crack developments are physical or mechanical problems is not convincing. Crystal defects (e.g. dislocations or micro-cracks) are not cracks? Small cracks grow into large cracks.

The above rejections were based on the combinations of references presented above. The fact that one of the individual references does not contain all of the claim limitations does not prove patentability. Motivation was given for the combinations made above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Anderson whose telephone number is (571) 272-1459. The examiner can normally be reached on M-F, 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Mills can be reached on (571) 272-1439. The

Art Unit: 1722

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAA
June 24, 2005


GREGORY MILLS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700